AMENDMENTS TO THE CLAIMS:

Please cancel Claims 11 through 16 without prejudice to or disclaimer of the subject matter recited therein.

1. (Previously Presented) A manufacturing method of manufacturing a semiconductor device having a plurality of wiring layers, said method comprising the steps of:

forming a wiring by a first wiring layer as a pattern by dividing a desired pattern into a plurality of patterns, connecting the divided patterns, and exposing them, wherein a position of the connection is formed in parallel with the wiring which is formed by the first wiring layer; and

forming a wiring by a second wiring layer having an area which intersects the connecting position by a batch processing of exposure.

2. (Previously Presented) A method according to claim 1, wherein the wiring which is formed by the first wiring layer does not have an area which overlaps the connecting position and the wiring which is formed by the second wiring layer has the area which overlaps the connecting position.

3. (Previously Presented) A method according to claim 1, wherein the first wiring layer is a horizontal direction wiring layer which is parallel with the connecting position for

connecting the divided patterns and the second wiring layer is a vertical direction wiring layer which perpendicularly crosses the connecting position.

4. (Previously Presented) A manufacturing method of manufacturing a solid state image pickup device having pixels each having a photoelectric converting area for converting light into signal charges and a plurality of wiring layers including a first wiring layer and a second wiring layer, said method comprising the steps of:

forming a wiring by the first wiring layer as a pattern by dividing a desired pattern into a plurality of patterns, connecting the divided patterns, and exposing them, wherein a position of the connection is arranged in parallel with the wiring which is formed by the first wiring layer; and

forming a wiring by the second wiring layer having an area which intersects the connecting position by a batch processing of exposure.

5. (Previously Presented) A method according to claim 4, wherein the wiring which is formed by the first wiring layer does not have an area which overlaps the connecting position for connecting the divided patterns and the wiring which is formed by the second wiring layer has the area which overlaps the connecting position.

6. (Previously Presented) A method according to claim 4, wherein a vertical direction wiring is formed by the first wiring layer, and a horizontal direction wiring is formed by the second wiring layer.

7. (Previously Presented) A method according to claim 6, wherein the horizontal direction wiring is a drive wiring of the pixels.

8. (Previously Presented) A method according to claim 4, wherein before the step of forming the plurality of wiring layers, a CMOS process is included at the time of the pixel creation.

9. (Previously Presented) A method according to claim 1, wherein alignment of the pattern for forming the first wiring layer and the pattern for forming the second wiring layer is made by a die-by-die system.

10. (Previously Presented) A method according to claim 4, wherein alignment of the pattern for forming the first wiring layer and the pattern for forming the second wiring layer is made by a die-by-die system.

11-16. (Cancelled)